IN THE CLAIMS

Claims 1-25 were in the original application.

Please cancel claims 1, 8, and 15.

Please amend claims 2-7, 9-14, and 16-25 as follows:

Please amend claims 2-7, 9-14, and 16-24 as follows:

A2

2 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (c.) is plasma-enhanced.

3 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (c.) uses TEOS as a source gas.

4 (Amended). The [method] integrated circuit of Claim [1] 22, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

5 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

6 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

7 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said interlevel dielectric is a doped silicate glass.

A3

9 (Amended). The [method] integrated circuit of Claim [8] 23, wherein said deposition step (c.) is plasma-enhanced.

10 (Amended). The [method] integrated circuit of Claim [8] 23, wherein said deposition step (c.) uses TEOS as a source gas.

11 (Amended). The [method] integrated circuit of Claim [8] 23, comprising the additional step of applying a passivating

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dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

A3 cont.

12 (Amended). The [method] integrated circuit of Claim [8] 9, 23, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

13 (Amended). The [method] integrated circuit of Claim [8] 9, 23, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

14 (Amended). The [method] integrated circuit of Claim [8] 9, 23, wherein said interlevel dielectric is a doped silicate glass.

A4

16 (Amended). The [method] integrated circuit of Claim [15] 15, 24, wherein said deposition step (c.) is plasma-enhanced.

17 (Amended). The [method] integrated circuit of Claim [15] 15, 24, wherein said deposition step (c.) uses TEOS as a source gas.

18 (Amended). The [method] integrated circuit of Claim [15] 15, 24, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19 (Amended). The [method] integrated circuit of Claim [15] 15, 24, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

20 (Amended). The [method] integrated circuit of Claim [15] 15, 24, wherein said interlevel dielectric is a doped silicate glass.

21 (Amended). The [method] integrated circuit of Claim [15] 15, 24, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

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~~22~~ (Amended). An integrated circuit manufactured by the method [of claim 1.] comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer, to produce a stack including said third dielectric layer over said first and second dielectric layers;
(e.) performing a global etchback to substantially remove portions of said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining third dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

~~23~~ (Amended). An integrated circuit manufactured by the method [of claim 8.] comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing silicon dioxide, to form a second dielectric layer over said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second layers;
(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated

structure, wherein at least a portion of said spin-on glass of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining spin-on glass of said third dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

Amend

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~~24~~ (Amended). An integrated circuit manufactured by the method [of claim 15.] comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer, said second dielectric layer having a thickness equal to or less than said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second dielectric layers, said third dielectric layer having a thickness equal to or greater than said second layer;
(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining second dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.